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ABSTRACT

Two planarization techniques for high aspect ratio three dimensional pillar structured P-I-N diodes have been developed in order to enable a continuous coating of metal on the top of the structures. The first technique allows for coating of structures with topography through the use of a planarizing photoresist followed by RIE etch back to expose the tops of the pillar structure. The second technique also utilizes photoresist, but instead allows for planarization of a structure in which the pillars are filled and coated with a conformal coating by matching the etch rate of the photoresist to the underlying layers. These techniques enable deposition using either sputtering or electron beam evaporation of metal films to allow for electrical contact to the tops of the underlying pillar structure. These processes have potential applications for many devices comprised of 3-D high aspect ratio structures.

Introduction

Three dimensional structures for micro- and nanoelectronics are under investigation for a number of uses. Applications include thermoelectrics [1,2], catalysts[3,4], and sensors[5,6]. These three dimensional structures may be filled, either with a functional material, such as a catalyst or sensing material, or else with a material for support, or electrical isolation. Figure 1 shows a schematic diagram of a representative device, with silicon p-i-n pillar diode. This structure is then coated with an functional or support material in order to create a three dimensional device. A functional material may be one which acts as a sensor or catalyst while a support material is defined as one which is not active in the device but is necessary for stability of the structure or for deposition of blanket coatings. We are currently investigating three dimensional P-I-N Si diode pillar arrays filled with isotopically enriched ^{10}Boron for thermal neutron detection.[7] In order to realize functionality of our devices, as well as similar three dimensional structures for other uses, it is necessary to make an electrical contact to the top of structure, which is the p+ layer of the diode. Achieving a blanket, conformal coating can be difficult due to topography across the device structure. Without methods to achieve this, a loss in device functionality will occur.

In this work, we have developed two techniques in order to achieve sufficiently planar surfaces over high aspect ratio pillars to allow conformal deposition of an electrode. Full wafer planarization has been done successfully by chemical mechanical polishing (CMP)[8,9]. However the aspect ratio of the features being planarized is typically small, in many cases with a ratio on the order of 1:1. Spin-on-glass (SOG) has also been developed for relatively shallow structures used for trench isolation, and interlayer metal interconnect. [10,11] SOG can have difficulties with cracking, gaps and surface smoothness[12] and low viscosity.[13] Some spin coating photoresist in conjunction with a plasma etch-back has also been used to planarize 2 µm deep trenches[14] and similarly tall nanowires.[155,166] Here we show methods to planarize high aspect ratio PIN diodes with an aspect ratio up to at least 24:1.

Planarization with Photoresist and Etch-Back

The first technique reported is applicable to both unfilled three dimensional structures, in which case a support material will be used that is not active in the device, and structures filled with a functional material. Samples for planarization were prepared by Deep Reactive Ion Etching (DRIE) in an STS Silicon Etcher. They were masked with photoresist using standard photolithographic processes in a 2 µm x 2 µm square pillar pattern with 2 µm spacing between pillars. Vertical pillars were etched to depths of 16, 28, and 45 µm to obtain aspect ratios of 8:1, 14:1, and 22:1.

Unfilled pillars were then coated using Shipley S1518 photoresist to fill in the etched areas as a support material. The S1518 was spun on using an initially slow speed of 500 rpm for 60s followed by a secondary, faster spin speed of either 1500, 2500, or 4000 rpm for 60s. The slow initial spin is necessary to spread the photoresist over the sample and allow it to leak into the etched areas while the higher speed spin results in a relatively uniform coating over the top of the pillars. Figure 2 shows the fill factor as a percentage of the pillar height vs number of spins for 28 µm pillars for varying secondary spin speeds. The fill factor is calculated as the percentage of the feature height filled by the photoresist. A secondary spin speed of 1000 rpm was not sufficient to achieve a planar coating of photoresist. All spin speeds examined yield a high fill factor after only three coatings, which is a reasonable number for such deep structures.

Figure 3 shows the fill factor as a percentage of pillar height vs number of spins for varying pillar heights with spin speed of 500/2500 rpm. Note that for all heights, only three spins is sufficient to achieve a high degree of filling. Figure 4 shows SEMs of the progression for 45 µm pillars.

Finally, it should be noted that hard baking the photoresist after each spin on a hotplate is necessary in order to maintain the integrity of the planarity after metal deposition. Baking conditions are: 75^{o}C for 60s, 95^{o}C for 120s, 110^{o}C for 120 s, and ramp to 200^{o}C and hold for 300s. Photoresist cured at only 120^{o}C or 150^{o}C displays a large number of cracks, which is prevented by bake at 200^{o}C.

A similar technique can be used to planarize pillars which are filled with a functional material, which could include materials such as SiO_2 or SiN_x, but for our application low pressure chemical vapor deposited (LPCVD) ^{10}Boron was used. Fabrication of these structures is described in previous work.[5] Because of the conformal nature of the ^{10}Boron deposition, the tops of the pillars are covered with a bump layer, shown in Figure 5a. It is necessary to remove this layer of ^{10}Boron in order to make electrical contact to the underlying Si devices, which is done using an electron cyclotron resonance (ECR) plasma etcher. Our ^{10}Boron etch process is reported separately.[17,18] However, due to the nature of this etch as well as the initial film morphology and nonuniformity across the sample, the resulting surface may possess topography that has a peak to valley distance on the order of 1 µm. Figure 5b shows a completed ^{10}Boron etch, with the pillar protruding out above the surrounding ^{10}Boron as well as low lying areas between pillars. Metallizing this structure can be problematic and can lead to both shorts and opens, if planarization is incomplete. If not enough photoresist is removed to uncover the tops of the pillars, no electrical contact to the underlying device is achieved. If too much is removed, the device is shorted and does not function properly. In both cases, the functionality of the device is compromised. While this process leaves photoresist on the device, we have not observed any penalty in device performance resulting from its presence. Figure 6 shows current density vs voltage (JV) plots for both shorted and properly functioning devices. Note the extremely high leakage current for the shorted device, a result of incomplete photoresist filling.

Following coating of either unfilled or partially filled pillar structures with a planarized photoresist, the next step is to etch back the photoresist to reveal the tops of the Si pillars. This is done using an O_2 Reactive Ion Etch (RIE) plasma. Figure 7 displays the progression from photoresist covered pillars to revealed pillar tops for (a,b) unfilled pillars and (c,d) partially filled pillars. By removing just enough photoresist to uncover the tops of the pillars, blanket metallization is possible. This allows for full device functionality to be achieved.

Planarization by Etch Rate Matching

The second approach involves the use of the same photoresist but spun on prior to ECR plasma etching. By matching the etch rate of the photoresist with the ^{10}Boron, a nearly flat surface without protruding pillar tops can be achieved. This is possible because variation in the photoresist thickness is minimal. For example, on bare Si pieces of this size, ignoring edge effects, the variation is less than 0.05 µm. This is an insignificant amount compared to the amount of variation across both the initial and final surfaces. The goal of this is to produce close to uniform pillar exposure across the detector area while significantly decreasing the divots between the pillars.

Figure 8 displays a schematic of our procedure. Prior to etching, an adhesion promoter HMDS and photoresist S1518 are spun onto detector samples using the same spin speed and bake as previously discussed. One coating is sufficient for this purpose and results in ~2 µm thick layer. Nanospec measurements taken on 1.5x1.5 cm^2 silicon samples spun under the same conditions show a variation in thickness over the samples of only ~ 0.025 µm.

It is necessary to obtain a photoresist coating that is continuous, without pinholes, and with minimal edge effects. Pinholes in the photoresist result in etch pits in the final surface and could result in shorting of the silicon pillar diodes. These etch pits can result in shorting of the pillar array if too deep or a non-continuous coating of final metal. They are the result of air expanding and escaping from the pillar structure during the final high temperature bake. It is thus necessary to remove this step. If edge effects extend to the detector area, thicker photoresist will result in uncovered pillars at the conclusion of the etch step. Edge effects can be minimized with careful application of photoresist during spin on.

After achieving a defect free, planar coating of photoresist, samples are inserted into the ECR plasma etcher. Etching of ^{10}Boron coated pillar structures has previously been reported.[17,18] A number of etch conditions have been examined in order to achieve a ^{10}Boron:S1518 selectivity of close to unity. Figure 9 shows the etch rates for ^{10}Boron and S1518 under the most promising etch conditions, which are 850W ECR power, 3 mTorr pressure, and 5 sccm SF_6. Etches were performed for 150 s. Due to the differing temperature dependences of the ^{10}Boron and S1518 etches, it is not possible to perfectly match the rates. Keeping etch times short enough to prevent significant heating during the etch is adequate to achieve a sufficiently smooth surface. Etching for longer times may result in alternate results due to increased differential etch rates due to heating during the etch. In addition, uniform thermal contact between the sample and the plate is necessary in order to prevent more rapid etching of localized areas that are not in good contact. The ^{10}Boron etch rate is ~0.55 µm /min at 500W. The etch rate for the S1518 is lower than that of ^{10}Boron at low powers, but increases to 99% of that of ^{10}Boron at 500W. This condition was chosen for the initial etch step.

Following the initial etch step to planarize the surface, O_2 is added to the plasma and etching is performed under the following conditions: 10 sccm SF_6, 20 sccm O_2, 3 mTorr, 200W RF, 850W ECR. Figure 10 shows the final etch surface of the pillar with etch matching planarization. Note the much smoother morphology of the improved etch using the etch matching technique.

Following the photoresist etch back, metal was deposited by a blanket, conformal coating. Because some amount of topography still exists, use of a wedge, planetary metal deposition system, or high pressure sputtering is preferred in order to ensure adequate coverage of the exposed sidewalls and thus a conformal coating. Coating with photoresist followed by an RIE plasma etch back allows for conformal metal coatings of structures which cannot be coated otherwise using physical deposition techniques. The continuous and conformal metal coating allow nearly all of the underlying P-I-N pillar structured diodes to be electrically active.

Conclusion

Two separate processes have been developed in order to ensure a uniform surface for deposition of an electrode on our ^{10}Boron filled P-I-N pillar structured diodes. Each uses S1518 photoresist in order to achieve a relatively uniform surface despite the non-uniformity of the underlying detector. Both processes allow for metallization of the final structure and provide good electrical continuity over a 3D pillar structure.

ACKNOWLEDGEMENTS

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FIGURE CAPTIONS

Figure 1. Schematic of filled three dimensional micro or nanostructure where A is the substrate material and B is the functional or support material.

Figure 2. Fill % as a function of secondary spin speed for varying pillar heights.

Figure 3. Fill % as a function of pillar height for constant spin speed

Figure 4. SEM images of 45 µm pillars after 1, 2, and 3 coats of photoresist.

Figure 5. ^{10}Boron filled structure (a) before and (b) after ECR plasma etching.

Figure 7. Progression from photoresist covered pillars to revealed pillar tops for (a,b). unfilled pillars and (c,d) ^{10}Boron filled pillars.

Figure 8. Schematic of planarizing by etch rate matching.

Figure 9. Etch rate and selectivity for ^{10}Boron and S1518 Photoresist.

Figure 10. Final detector morphology with etch matched planarization

Figure 1

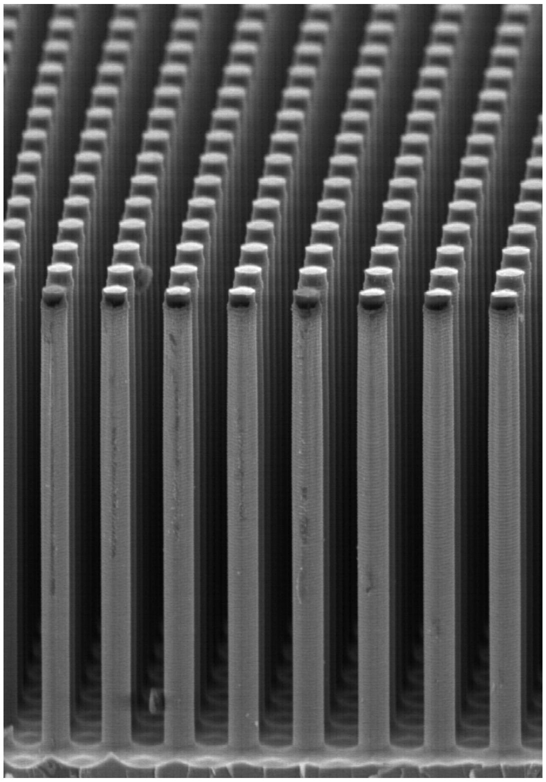

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Figure 2

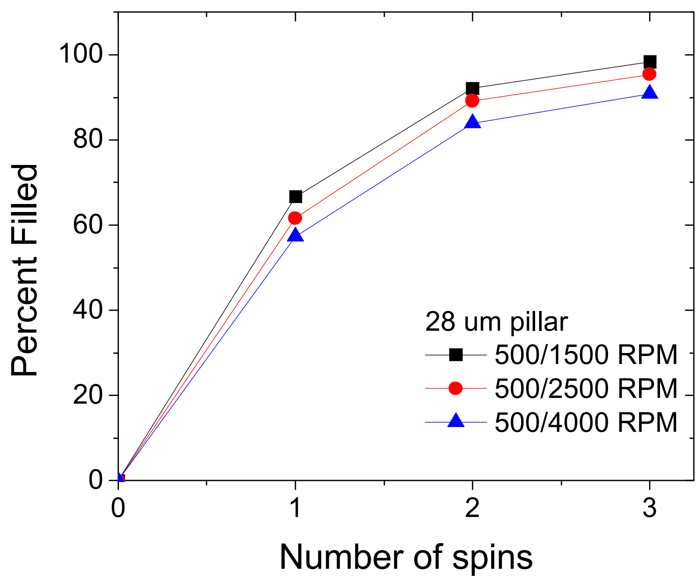

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Figure 3

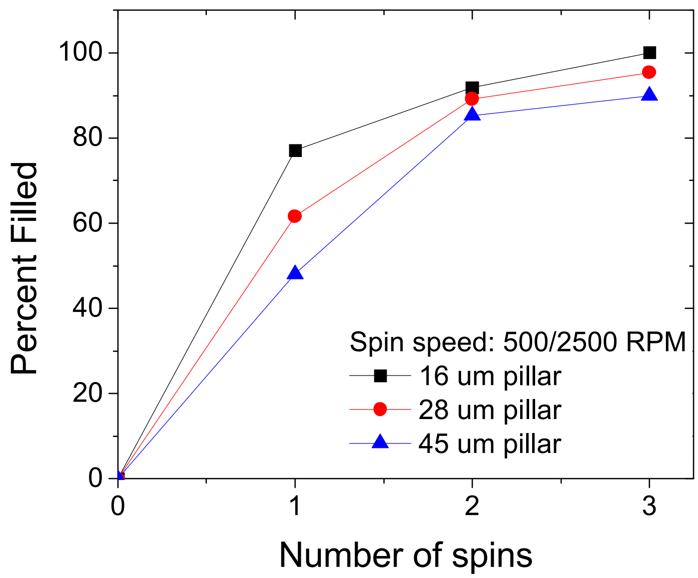

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Figure 4

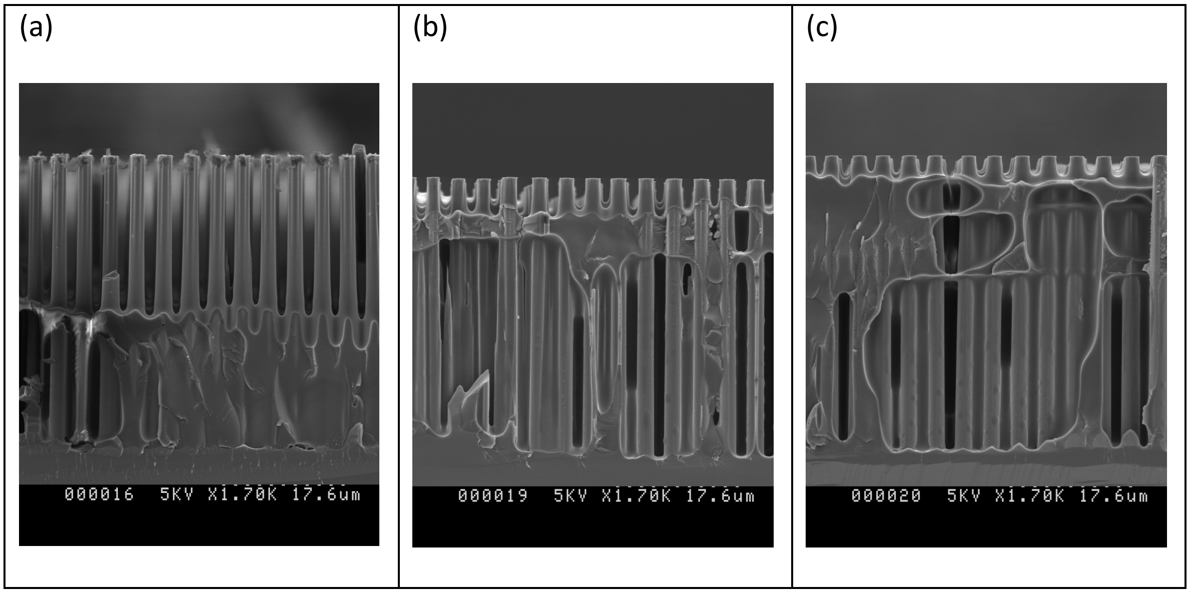
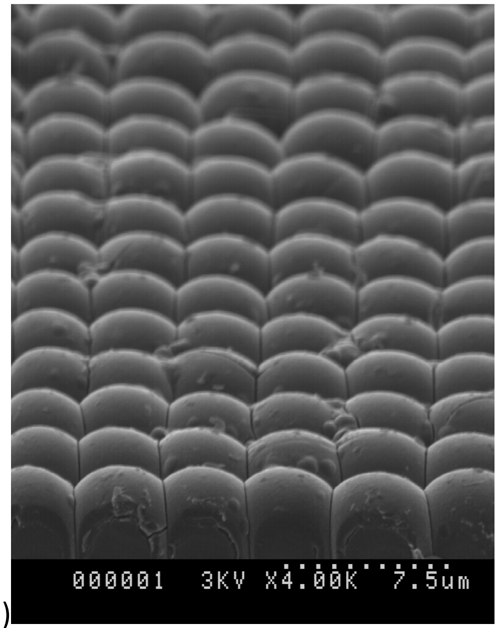
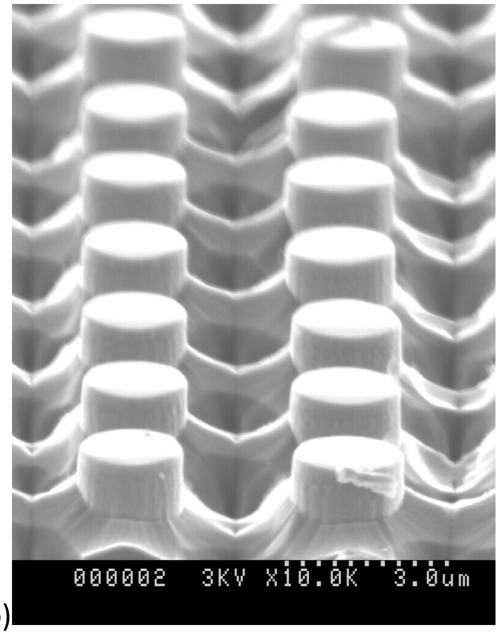

(a)
000016 5KV X1.70K 17.6um
(b)
000019 5KV X1.70K 17.6um
(c)
000020 5KV X1.70K 17.6um

Figure 5



(a)



(b)

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Figure 6

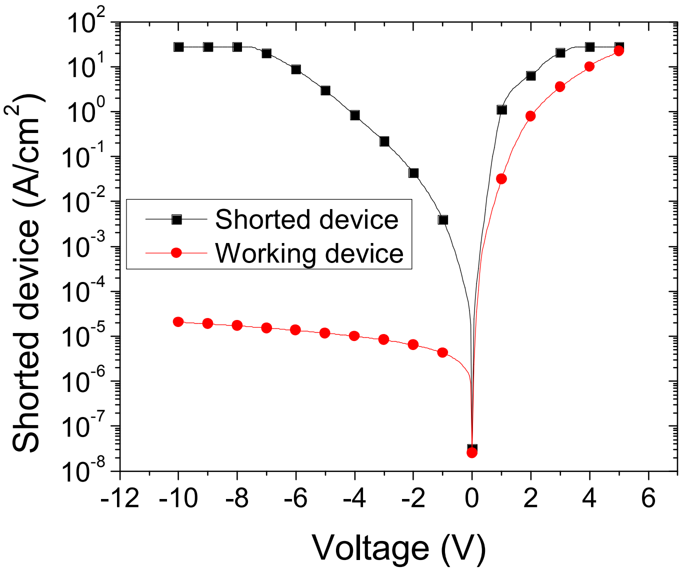

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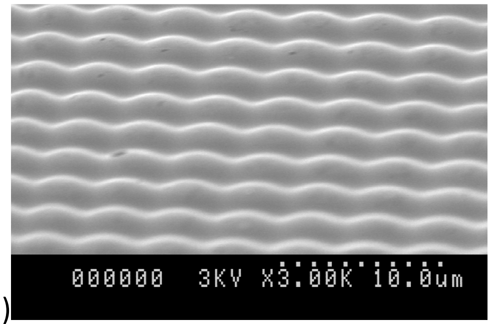
Figure 7



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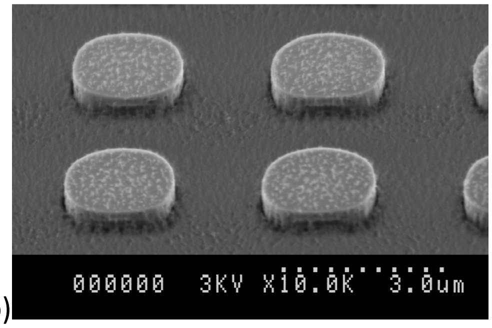

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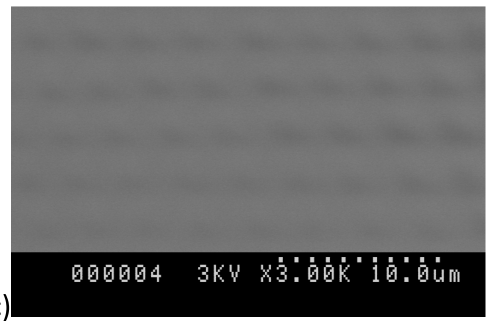

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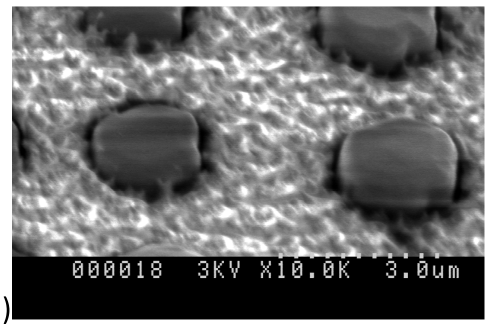

(d)

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Figure 8

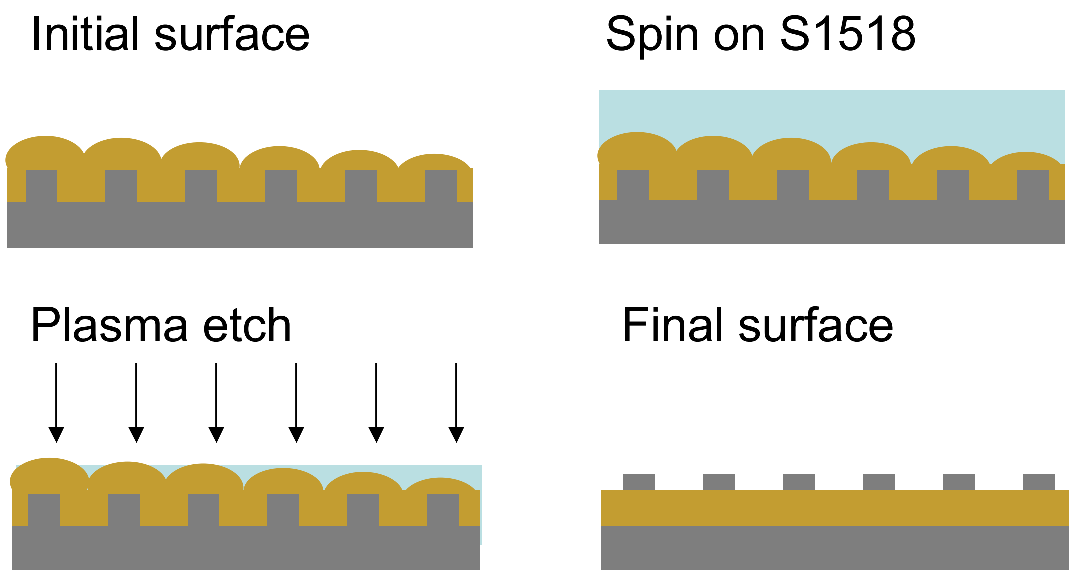

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Figure 9

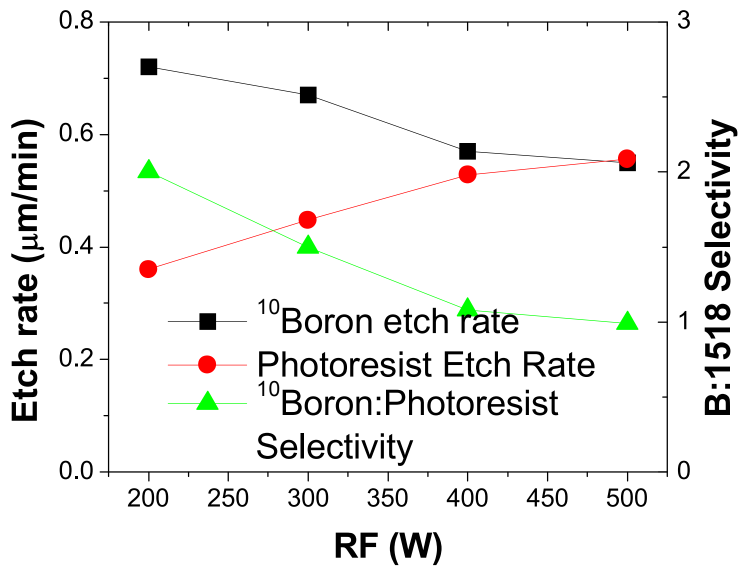

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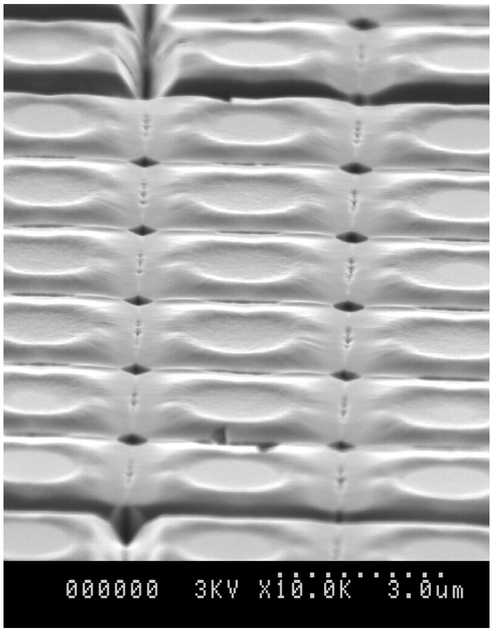
Figure 10



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